Docket No.: P2002,0618

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant

VERONIKA POLEI ET AL.

Filed

CONCURRENTLY HEREWITH

Title

METHOD FOR FABRICATING A BURIED BIT LINE FOR A

SEMICONDUCTOR MEMORY

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

Sir:

In accordance with 37 C.F.R. 1.98 copies of the following patents and/or publications are submitted herewith:

- U.S. Patent No. 6,326,268 B1 (Park et al.), dated December 4, 2001;
- U.S. Patent No. 6,242,305 B1 (Foote et al.), dated June 5, 2001;
- U.S. Patent No. 6,172,396 B1 (Chang), dated January 9, 2001;
- U.S. Patent No. 5,966,603 (Eitan), dated October 12, 1999;
- U.S. Patent No. 5,841,163 (Joo et al.), dated November 24, 1998;
- U.S. Patent No. 5,545,907 (Maari), dated August 13, 1996;
- U.S. Patent No. 5,168,334 (Mitchell et al.), dated December 1, 1992;
- U.S. Patent No. 4,947,222 (Gill et al.), dated August 7, 1990;

U.S. Patent No. 6,011,725 (Eitan), dated January 4, 2000;

U.S. Patent No. 5,768,192 (Eitan), dated June 16, 1998;

PCT WO 99/60631 (Eitan), dated November 25, 1999.

Respectfully submitted

For Applicants

Date: July 21, 2003

LAURENCE A. GREENBERG REG. NO. 29,308

Lerner and Greenberg, P.A. Post Office Box 2480

Hollywood, FL 33022-2480

Tel: (954) 925-1100 Fax: (954) 925-1101

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PATENT AND TRADEMARK OFFICE				Applicant: VERONIKA POLEI ET AL.					
INFORMATION DISCLOSURE STATEMENT BY APPLICANT									
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	Α	6,326,268 B1	12/4/01	Park et al.	OLAGO	CLASS		116	
	В	6,242,305 B1	6/5/01	Foote et al.					
	С	6,172,396 B1	1/9/01	Chang					
	D	5,966,603	10/12/99	Eitan					
	E	5,841,163	11/24/98	Joo et al.					
	F	5,545,907	8/13/96	Maari					
	G	5,168,334	12/1/92	Mitchell et al.					
	Н	4,947,222	8/7/90	Gill et al.					
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